

## REMARKS

This amendment responds to concerns raised by Examiner Ngyuen by telephone on 22 November 2004 and 10 December 2004. First off, I wish to thank Examiner Ngyuen not only for taking the time to discuss this case with me, but also for his careful reading of the claims.

In summary, the Examiner stated that the recitations in the original claim 1 relating to the number of address bits in the first and second identifiers were either confusing or incorrect. In particular, it needed to be made clear that the identifiers (typically, addresses) used by the device to access the memory are shorter (have fewer bits) than those used by the I/O-initiating subsystem. For example, the invention makes it possible for I/O subsystems that use 64-bit addresses to pass data via low memory to and from a device that may use only 32-bit addresses.

The examiner also stated that it should be made clear in claim 1 that the memory is a *hardware* memory. Also, the Examiner observed that the phrase "the buffer" in claim 3 lacked antecedent basis. Claims 1 and 3 have been amended accordingly.

For the same reasons as related to claim 1, the Examiner required amendment of the Summary of the Invention section of the specification, and the Abstract, so that they would conform to the corrected, amended wording of claim 1. This amendment does so, without adding any new matter.

Finally the Examiner required a terminal disclaimer because of alleged double-patenting in view of the issued parent application, U.S. Patent No. 6,725,289. Such a disclaimer is enclosed.

This application should now be in condition for allowance. If not, then I respectfully request an opportunity for yet another constructive telephone conversation with the Examiner. Thank you.

Date: 15 December 2004

Respectfully submitted,



34825 Sultan-Startup Rd.  
Sultan, WA 98294  
Phone & fax: (360) 793-6687  
pearce@vmware.com

Jeffrey Pearce  
Reg. No. 34,729  
Attorney for the Applicant(s)